REMARKS

Claims 23-110 are pending in this case. Based upon the following remarks, it is respectfully submitted that these claims are allowable.

Claims 23-110 were provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 23-152 of copending application no. 10/784,835. This rejection is respectfully traversed.

According to the Examiner, claims 23-110 of the instant application and claims 23-152 of copending application no. 10/784,835 are not patentably distinct from each other "because both apparatuses are [sic] still operate in the same manner when the control circuit receives control signals either internally ('local control signals' as claimed in the instant application) or externally ('incoming control signals' as claimed in 10/784,835[])." First, it is respectfully submitted that it should be noted that neither of the terms "internally" or "externally" is used in any of the present claims. Second, it is further respectfully submitted that the Examiner has improperly focused only upon the recited "control circuitry" elements, each of which is only one of multiple elements recited in each claim, while disregarding other elements such as the recited "plurality of subcircuits" which includes "pipeline subcircuitry" and is expressly recited as having distinct characteristics or features.

More specifically, independent claim 23 of the instant application reads as follows (with emphasis added):

> An apparatus including integrated processor circuitry, said apparatus comprising:
>
> a plurality of interface electrodes to convey at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

a plurality of subcircuits coupled to at least a portion of said plurality of interface electrodes and including pipeline subcircuitry responsive to a first clock signal having active and inactive states by selectively operating on one or more of said plurality of incoming instructions for data processing, wherein

a first portion of said pipeline subcircuitry is responsive to said active first clock signal by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of said one or more of said plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to said power management instruction, and

a second portion of said pipeline subcircuitry is coupled to said first pipeline subcircuitry portion and responsive to said active first clock signal by executing said one or more decoded instructions;

control circuitry coupled to said plurality of subcircuits and responsive to said one or more local control signals by providing one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to said one or more first selected assertion and de-assertion states of said one or more local control signals with said second selected assertion and de-assertion states following reception of said power management instruction; and

clock circuitry coupled to said control circuitry and said plurality of subcircuits, and responsive to said one or more clock control signals by providing at least said first clock signal with said first clock signal inactive

state corresponding to said one or more second selected assertion and de-assertion states of said one or more clock control signals.

Hence, the "power management instruction", which arrives via the "plurality of interface electrodes", is processed, e.g., decoded, by the "first portion of said pipeline subcircuitry" to provide the "one or more local control signals" which, in turn, affect the "one or more clock control signals".

Meanwhile, independent claim 23 of copending application no. 10/784,835 reads as follows (with emphasis added):

An apparatus including integrated processor circuitry, said apparatus comprising:

a plurality of interface electrodes including one or more control electrodes to convey one or more incoming control signals from at least one signal source having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

control circuitry coupled to said one or more control electrodes and responsive to said one or more incoming control signals by providing at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states with said respective assertion states following said first incoming control signal states combination;

clock circuitry coupled to said control circuitry and responsive to said at least one clock control signal by providing at least a first clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively; and

a plurality of subcircuits coupled to at least a portion of said plurality of interface electrodes, said control circuitry and said clock circuitry, and including pipeline subcircuitry responsive to said first clock

plurality of interface electrodes, said control circuitry and said clock circuitry, and including pipeline subcircuitry responsive to said first clock signal by selectively operating on one or more instructions for data processing, wherein

a first portion of said pipeline subcircuitry is responsive to said active first clock signal by performing at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions to provide one or more decoded instructions, and

a second portion of said pipeline subcircuitry is coupled to said first pipeline subcircuitry portion and responsive to said active first clock signal by executing said one or more decoded instructions.

Hence, the "one or more incoming control signals", which arrive via the "plurality of interface electrodes", affect the providing of the "at least one clock control signal" by the "control circuitry". No portion of the "plurality of subcircuits", including any portion of the "pipeline subcircuitry", is expressly recited as playing a role in the providing of any form of clock control signal. While such a role is not necessarily excluded by the language of this claim, at the same time such a role is also not necessarily suggested. Therefore, it is respectfully submitted that patentably distinct differences exist between claims 23-110 of the instant application and claims 23-152 of copending application no. 10/784,835.

B. Consideration of Reference

On April 19, 2004, an Information Disclosure was timely filed with a Form PTO/SB/08A (02-03) listing, among others, pending U.S. patent application no. 10/784,396. (A copy of this form with the word "COPY" appearing in the top and

bottom margins is submitted herewith.) While the Examiner may have considered such reference, no initials appear in the column entitled "Examiner Initials" to indicate such consideration. The Examiner is respectfully requested to consider such reference and provide another copy of the Form PTO/SB/08A (02-03) with the initials of the Examiner included.

C. Conclusion

Claims 23-110 remain pending in this case. Based upon the foregoing remarks, it is respectfully submitted that these claims are allowable, and reconsideration and early allowance of these claims are requested.

Respectfully submitted,
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